REMARKS

Claims 1-23 were previously pending in this patent application. Claims 17-23 were withdrawn from further consideration pursuant to 35 U.S.C. Section 121. Claims 1-16 stand rejected. Herein, Claims 1 and 9 have been amended. Claims 4 and 12 have been cancelled. Accordingly, after this Amendment and Response, Claims 1-3, 4-11, and 13-16 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

DRAWINGS

On 8/25/04, seven sheets (i.e., sheet 1, sheet 2, sheet 3, sheet 4, sheet 5, sheet 6, and sheet 7) of formal drawings were submitted. A review of the seven sheets of formal drawings has discovered that sheet 6 including Figure 4B and sheet 7 including Figure 4C incorrectly depict the original informal drawings submitted on 9/04/2003. Herein, Figure 4B has been changed so that the label 20 is attached to the floating gate comprising the doped Poly1 (85) and the undoped Poly1 (80) as in the original informal drawings submitted on 9/04/2003. Further, Figure 4C has been changed so that the grains (89) are depicted as in the original informal drawings submitted on 9/04/2003. No new matter was added.

35 U.S.C. Section 103(a) Rejections

Claims 1-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPR) and Eom, U.S. Patent No. 5,817,547 (hereafter Eom). These rejections are respectfully traversed.

Independent Claim 1 recites:

> A method of fabricating a floating gate for a semiconductor device, said method comprising:
> depositing an undoped polycrystalline silicon layer on a tunnel oxide layer, wherein said undoped polycrystalline silicon layer has a first thickness;
> depositing a doped polycrystalline silicon layer on said undoped polycrystalline silicon layer, wherein said doped polycrystalline silicon layer has a second thickness, and wherein said undoped polycrystalline silicon layer and said doped polycrystalline silicon layer form said floating gate having a third thickness, ***wherein said doped polycrystalline silicon layer includes dopant material throughout said second thickness***; and
> ***performing a plurality of thermal processes such that said floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon.*** (emphasis added)

It is respectfully asserted that the combination of AAPR and Eom does not disclose the present invention as recited in Independent Claim 1. The Office Action (at page 3) cites several portions of AAPR and Eom to support the rejections under 35 U.S.C. 103(a). To the contrary, the combination of AAPR and Eom is directed to a method unlike the method recited in Independent Claim 1. In particular, AAPR discloses a method of fabricating a floating gate, wherein the method includes depositing a doped polycrystalline silicon layer. Further, Eom is directed to method of fabricating a MOSFET gate, wherein the method includes forming a first polysilicon layer (13) and subsequently forming a second polysilicon layer (14) doped with impurities on the first polysilicon layer (13). [Eom; Col. 3, lines 45-57]. However, Eom clearly states that only the upper or the lower one third of the second polysilicon layer (14) is doped with impurities. [Eom; Col. 3, lines 58-65]. Also, Eom states that, alternatively, only the middle part of the second polysilicon layer (14) is doped with impurities. Id. That is, Eom teaches away from using a second polysilicon layer that is doped with impurities throughout the second polysilicon layer. Thus, the combination of AAPR and Eom fails to disclose depositing an undoped polycrystalline silicon layer and depositing a doped polycrystalline silicon layer on the undoped polycrystalline silicon layer, wherein the doped polycrystalline silicon layer includes dopant material throughout the thickness of the doped polycrystalline silicon layer. Furthermore, the combination of AAPR and

Eom fails to disclose performing a plurality of thermal processes such that the floating gate (formed by the undoped polycrystalline silicon layer and the doped polycrystalline silicon layer) comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon.

Unlike the combination of AAPR and Eom, Independent Claim 1 is directed to a method of fabricating a floating gate for a semiconductor device. The method comprises depositing an undoped polycrystalline silicon layer on a tunnel oxide layer, wherein the undoped polycrystalline silicon layer has a first thickness. Further, the method includes depositing a doped polycrystalline silicon layer on the undoped polycrystalline silicon layer, wherein the doped polycrystalline silicon layer has a second thickness, and wherein the undoped polycrystalline silicon layer and said doped polycrystalline silicon layer form the floating gate having a third thickness, wherein the doped polycrystalline silicon layer includes dopant material throughout the second thickness. Also, the method comprises performing a plurality of thermal processes such that the floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon. As described above, the combination of AAPR and Eom does not disclose the cited claim limitations of Independent Claim 1. Therefore, it is respectfully submitted

that Independent Claim 1 is patentable over the combination of AAPR and Eom and is in condition for allowance.

Dependent Claims 2-3 and 5-8 are dependent on allowable Independent Claim 1, which is allowable over the combination of AAPR and Eom. Hence, it is respectfully submitted that Dependent Claims 2-3 and 5-8 are patentable over the combination of AAPR and Eom for the reasons discussed above.

With respect to Independent Claim 9, it is respectfully submitted that Independent Claim 9 recites similar limitations as in Independent Claim 1. In particular, Independent Claim 9 is directed to a method of fabricating a stacked gate structure for a semiconductor device. The method comprises forming a tunnel oxide layer on a surface of a semiconductor substrate, depositing an undoped polycrystalline silicon layer on the tunnel oxide layer, wherein the undoped polycrystalline silicon layer has a first thickness. Further, the method includes depositing a doped polycrystalline silicon layer on the undoped polycrystalline silicon layer, wherein the doped polycrystalline silicon layer has a second thickness, and wherein the undoped polycrystalline silicon layer and the doped polycrystalline silicon layer form a floating gate having a third thickness, wherein the doped

polycrystalline silicon layer includes dopant material throughout the second thickness. Also, the method includes performing a plurality of thermal processes such that the floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon. Furthermore, the method comprises forming a ONO (Oxide-Nitride-Oxide) layer on the floating gate and forming a control gate on the ONO layer. As described above, the combination of AAPR and Eom does not disclose the cited claim limitations of Independent Claim 9. Therefore, Independent Claim 9 is allowable over the combination of AAPR and Eom for reasons discussed in connection with Independent Claim 1.

Dependent Claims 10-11 and 13-16 are dependent on allowable Independent Claim 9, which is allowable over the combination of AAPR and Eom. Hence, it is respectfully submitted that Dependent Claims 10-11 and 13-16 are patentable over the combination of AAPR and Eom for the reasons discussed above.

Claims 1-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPR) and Schuegraf et al., U.S. Patent Application Publication No. US 2002/0086503 (hereafter Schuegraf). These rejections are respectfully traversed.

It is respectfully asserted that the combination of AAPR and Schuegraf does not disclose the present invention as recited in Independent Claim 1. The Office Action (at page 4) cites several portions of AAPR and Schuegraf to support the rejections under 35 U.S.C. 103(a). To the contrary, the combination of AAPR and Schuegraf is directed to a method unlike the method recited in Independent Claim 1. In particular, AAPR discloses a method of fabricating a floating gate, wherein the method includes depositing a doped polycrystalline silicon layer. Further, Schuegraf is directed to method of fabricating a transistor, wherein the method includes forming a substantially undoped silicon-comprising layer (40), subsequently forming a conductively doped silicon-comprising layer (42) over the substantially undoped silicon-comprising layer (40), and subjecting the substantially undoped silicon-comprising layer (40) and the conductively doped silicon-comprising layer (42) to an anneal to activate dopant, as well as diffuse dopant from heavily doped layer (42) into substantially undoped layer (40) . [Schuegraf; paragraphs [0059-0062]]. However, Schuegraf fails to disclose performing a plurality of thermal processes such that the floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon. In fact, Schuegraf never discusses grain size. Thus, the combination of AAPR and Schuegraf fails to disclose performing a plurality of thermal processes

such that the floating gate (formed by the undoped polycrystalline silicon layer and the doped polycrystalline silicon layer) comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon.

Unlike the combination of AAPR and Schuegraf, Independent Claim 1 is directed to a method of fabricating a floating gate for a semiconductor device. The method comprises depositing an undoped polycrystalline silicon layer on a tunnel oxide layer, wherein the undoped polycrystalline silicon layer has a first thickness. Further, the method includes depositing a doped polycrystalline silicon layer on the undoped polycrystalline silicon layer, wherein the doped polycrystalline silicon layer has a second thickness, and wherein the undoped polycrystalline silicon layer and said doped polycrystalline silicon layer form the floating gate having a third thickness, wherein the doped polycrystalline silicon layer includes dopant material throughout the second thickness. Also, the method comprises performing a plurality of thermal processes such that the floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon. As described above, the combination of AAPR and Schuegraf does not disclose the cited claim limitations of Independent Claim 1. Therefore, it is respectfully

submitted that Independent Claim 1 is patentable over the combination of AAPR and Schuegraf and is in condition for allowance.

Dependent Claims 2-3 and 5-8 are dependent on allowable Independent Claim 1, which is allowable over the combination of AAPR and Schuegraf. Hence, it is respectfully submitted that Dependent Claims 2-3 and 5-8 are patentable over the combination of AAPR and Schuegraf for the reasons discussed above.

With respect to Independent Claim 9, it is respectfully submitted that Independent Claim 9 recites similar limitations as in Independent Claim 1. In particular, Independent Claim 9 is directed to a method of fabricating a stacked gate structure for a semiconductor device. The method comprises forming a tunnel oxide layer on a surface of a semiconductor substrate, depositing an undoped polycrystalline silicon layer on the tunnel oxide layer, wherein the undoped polycrystalline silicon layer has a first thickness. Further, the method includes depositing a doped polycrystalline silicon layer on the undoped polycrystalline silicon layer, wherein the doped polycrystalline silicon layer has a second thickness, and wherein the undoped polycrystalline silicon layer and the doped polycrystalline silicon layer form a floating gate having a third thickness, wherein the doped

polycrystalline silicon layer includes dopant material throughout the second thickness. Also, the method includes performing a plurality of thermal processes such that the floating gate comprises a plurality of grains, each grain being smaller than the grains of a floating gate formed using only doped polycrystalline silicon. Furthermore, the method comprises forming a ONO (Oxide-Nitride-Oxide) layer on the floating gate and forming a control gate on the ONO layer. As described above, the combination of AAPR and Schuegraf does not disclose the cited claim limitations of Independent Claim 9. Therefore, Independent Claim 9 is allowable over the combination of AAPR and Schuegraf for reasons discussed in connection with Independent Claim 1.

Dependent Claims 10-11 and 13-16 are dependent on allowable Independent Claim 9, which is allowable over the combination of AAPR and Schuegraf. Hence, it is respectfully submitted that Dependent Claims 10-11 and 13-16 are patentable over the combination of AAPR and Schuegraf for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above amendments, arguments and remarks overcome all rejections and objections. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-3, 5-11, and 13-16) are in condition for allowance.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

Wagner, Murabito & Hao, LLP

Dated: 1/25/2005

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Attachments

Amendments to the Drawings:

On 8/25/04, seven sheets (i.e., sheet 1, sheet 2, sheet 3, sheet 4, sheet 5, sheet 6, and sheet 7) of formal drawings were submitted. A review of the seven sheets of formal drawings has discovered that sheet 6 including Figure 4B and sheet 7 including Figure 4C incorrectly depict the original informal drawings submitted on 9/04/2003. Herein, Figure 4B has been changed so that the label 20 is attached to the floating gate comprising the doped Poly1 (85) and the undoped Poly1 (80) as in the original informal drawings submitted on 9/04/2003. Further, Figure 4C has been changed so that the grains (89) are depicted as in the original informal drawings submitted on 9/04/2003.

Attachment: Replacement Sheet for Figure 4B

Annotated Sheet for Figure 4B

Replacement Sheet for Figure 4C

Annotated Sheet for Figure 4C

ANNOTATED SHEET

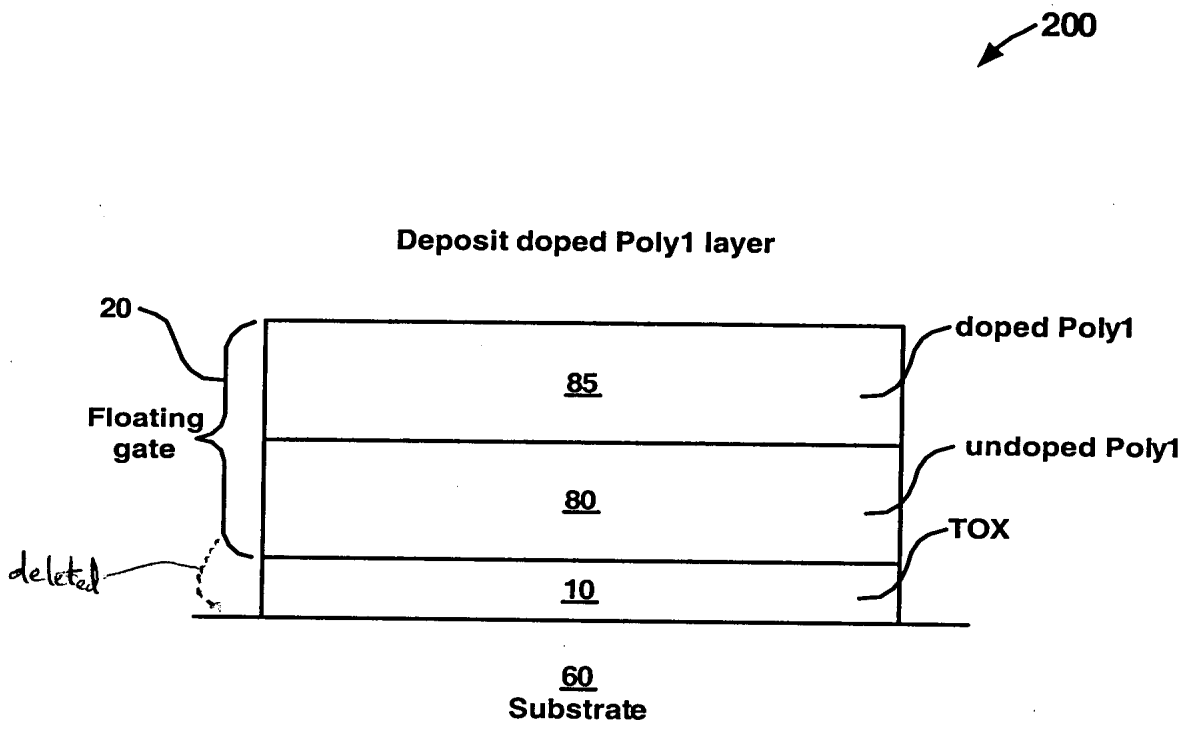

FIG. 4B

ANNOTATED SHEET

After thermal processes have been performed

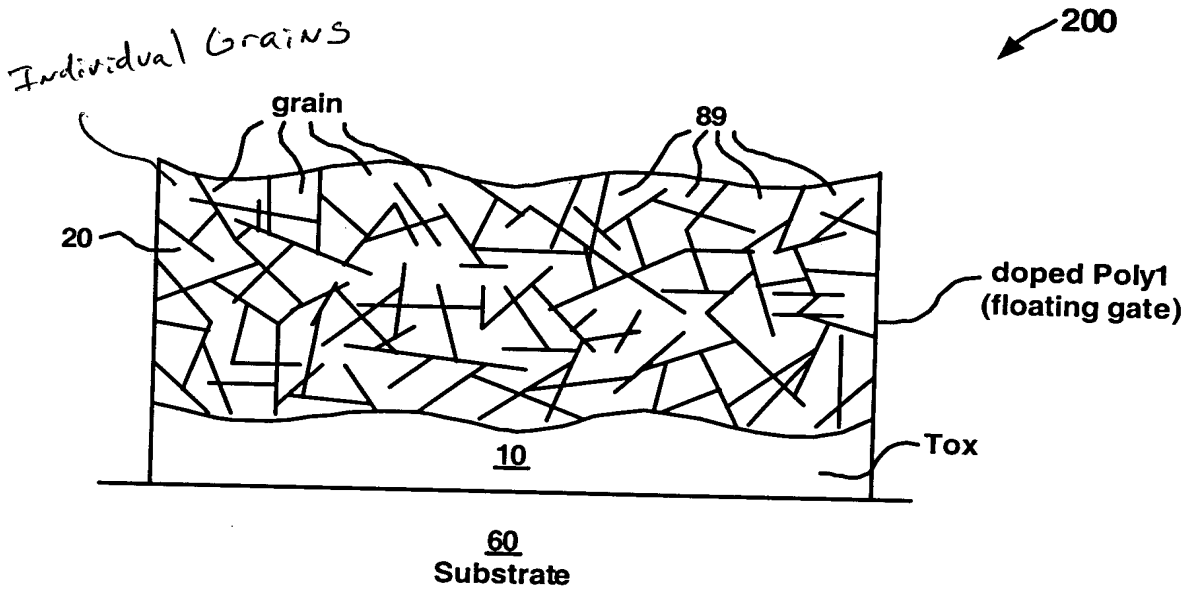

FIG. 4C